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C. IRVIN MCCLELLAND
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
SAXENA, AKASH	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,583	MITROVIC, ANDREJ S.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/9/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-65 has/have been presented for examination based on amendment filed on 26th May 2006.
2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9th June 2006 has been entered.
3. Claim(s) 1, 28 and 55 are amended.
4. Claim(s) 63-65 are new claim(s) added with this amendment.
5. The arguments submitted by the applicant have been fully considered. Claims 1-65 remain rejected. The examiner's response is as follows.

Response to Applicant's Remarks for Double Patenting

6. Examiner acknowledges applicant's intent to filing a terminal disclaimer for applications 10/673,501, 10/673,507 and 10/673,138 are considered and double patenting rejection is maintained until a terminal disclaimer is filed. Claim amendment as presented in these application mirrors the amendments in the current application.

Response to Applicant's Remarks for 35 U.S.C. § 103

6. **Claims 1-44 were rejected under 35 U.S.C. 103(a) as being unpatentable over Sonderman, in view of Jain.**

Regarding Claim 1-44

Applicant has argued that

> First, Sonderman et al fail to disclose or suggest a first principles physical model including a set of computer-encoded differential equations or performing first principles simulation for the actual process being performed...In the present case, there appears to be disagreement between the Applicant and the examiner as to whether or not Sonderman et al discloses or suggests the claimed first principles physical model by their disclosure of a device physics model, process model, and an equipment model.

Applicant submits the article "1999 Casting Simulation Software Survey" (Referred to as Midea reference hereafter) as identifying three types of simulations, namely, Empirical, Semi Empirical, and Physics based first principle programs that require complex mathematical and accurate material thermo physical data. This article is used to distinguish the current application from the prior art and further defining the first principle simulation as not the "empirical" or "semi empirical" simulation but "Physics based first principles" simulation.

Examiner asserts that Sonderman and Jain reference provides "Physics based first principles" simulation as disclosed in the submitted article. The reason is set as forth.

Midea teaches first principles simulation as:

> In first principles programs, complex physical relationships and equations are used along with detailed material physical data. The problem must be broken into small calculations via either a finite differencing method or a finite element method. This allows for calculations profile process changes as a function of time.

Using the mold filling example Midea states:

> Mold filling can be predicted using a first principles program. An approach is to employ Navier-stokes flow equations with a two-equation turbulence model. This approach accounts for all relevant flow characteristics (such ms viscosity, friction, Reynold's Number, etc.) in all spatial degrees of freedom. Continuity and the conservation of momentum and energy equations form the basis of these algorithms. This approach is accurate and has been time-tested in the aerospace industry for decades.

As seen above Maeda reference teaches first principles program using complex equations and finite difference methods and as example shows use of Navier-stokes flow equations.

Jain also teaches first principle simulation using complex physical relationships like Navier-stokes flow equations, Maxwells equations for electromagnetic effect. Helmhotlz's Equation for resonant structures, Poisson's equation for steady state temperature and Schroedinger equation for particles in potential field, to name a few used to model various simulations (Jain: Pg. 367-368 Section "Governing Rationale" Sub-Section A. Governing Equations; types of simulation that may cover the three models disclosed by Sonderman).

Further, Jain teaches the first principles simulation, similar to Maeda, because it uses the finite differencing method (Jain: Pg. 368-370 Section "Governing Rationale" Sub-Sections "Finite Difference Method" "Details of Finite Difference Method"). Hence Jain does not fall under the simple empirical or semi-empirical models as described by Maeda but under the "Physics based first principles" of Maeda.

Further, Jain use of the Mathematic Physical Engine (MPE) to simulate semiconductor wafers (Jain Abstract) where at least the fluid flow simulation, thermal flow simulation, diffusion process simulation, chemical Ion exchange simulation, vibration simulation, magnetic simulation and electromagnetic simulation can be

applied to the Sonderman's device physics model, process model, and an equipment model.

Secondly, Sonderman does not disclose use of tables of experimental results, rules and physical and guidelines and physical and algebraic equations to model physical process instead teaches cascading complex computation of values based on changes from one model to another (Sonderman: Col.6 Lines 1-16). This indicates that these models cannot be empirical or semi empirical models alone. Sonderman further indicates presence of detailed material physical data (as indicated by from Maeda above) in device physics model where the chemical reactions are modeled with oxide growth emulation (Sonderman: Col.5 Lines 48-55).

Therefore examiner disagrees that Sonderman-Jain combination does not teach the first principles simulation model.

Further, Applicant also points out that the Sonderman discloses statistical response function as denoted by equations 1 & 2 on Col.9.

Examiner agrees with the applicant, however this is not related to the simulation. The Fig.8 being referred to shows a simple feedback process control model of any system (semiconductor manufacturing system here) and not the simulation system. The input Xti to the actual semiconductor manufacturing system takes into account this statistical feedback as well as simulation (which is based on the actual runs of the semiconductor wafer Si - and not statistical runs). Col.9 Lines 46-51 States:

> The new control inputs, X.sub.Ti, are generally based upon a plurality of factors, such as simulation data, output requirements, product performance requirements, process recipe settings based on a plurality of processing tool 120 operating scenarios, and the like.

Indicating that simulation data is only one of the inputs to the actual semiconductor manufacturing system represented by Fig. 8 & Col.9. Therefore applicant's argument that simulation is based on the statistical response function is unfounded.

Applicant argues that:

> Another question with regard to the first point is whether Sonderman et al disclose providing simulation results for an actual process being performed.

Examiner is unclear if the applicant intentions are to argue temporal sequence between the simulation and actual process being performed. It seems that applicant intends to perform the simulation in parallel with the actual processing that is being performed. If this is the intention, the claim limitation stating, "***using the first principle simulation result to facilitate the actual process being performed by semiconductor processing tool***", ***contradicts*** *the intentions* as clearly the simulation results are used as input to the semiconductor processing performing actual processing.

As stated above Sonderman clearly disclose providing simulation results for an actual process being performed (Sonderman: Col.9 Lines 46-51 States).

Further to point out the difference that Sonderman is not providing simulation results for an actual process being performed applicant has pointed out to Col. 5-7. *Regarding Col.6 Lines 35-47:* Applicant has noted that simulation is performed and then the simulation data is passed on the process control. Also noted process control is based on the pre-existing simulation. However, examiner asserts that applicant is providing the arguments in support of the prior art teaching the claimed invention as simulation is performed in the step of "performing first principle

simulation ..." and then the results are applied the to actual processing in the step of "using the first principle simulation result to facilitate the actual processing...".

If the intention is that first simulation is not for the process being performed, Sonderman teaches in Col.3 Lines 56-63:

> The process control environment 180 controls the operations of the manufacturing environment 170. In one embodiment, the process control environment comprises an APC framework. The process control environment 180 can receive data from the manufacturing environment 170 and the simulation environment 210 and make appropriate changes to manufacturing control parameters to affect the operations of the manufacturing environment 170.

Further Sonderman states Col.7 Lines 4-7 states:

> Using the validated models, the simulation environment 210 can emulate the operations of an actual process control environment 180 that is integrated with a manufacturing environment 170.

Regarding Col.6 Lines 64-Col.7 Line 7: Applicant presumes that the model validation is based on the historical process data. Examiner respectfully disagrees, Sonderman states that the model validation is defined as **integration** of the "device physics model 310, the process model 320, and the equipment model 330, into a single manufacturing unit that is controlled by the simulator 340." Please see Col.6 Line 67-Col.7 Line 4. If one would infer any other form of validation, although not stated by Sonderman, Jain teaches model validation/verification using the first principle simulation MPE methodology (Jain: Pg.367 "Significance" point 1).

Regarding Col.7 Lines 8-20: Applicant has noted that Sonderman does not perform simulation of the actual manufacturing process; otherwise he would not have stated that "*as if* actual manufacturing process were being performed".

Examiner respectfully disagrees with applicant again, as Sonderman ***is*** performing the *simulation of a manufacturing process* ***not*** *an actual manufacturing process.*

Therefore the word "as if" makes sense. Further in light of the claim limitations being

contradictory to what is being argued. Sonderman is running simulation based on the same input as would be provided to the actual manufacturing process. Examiner disagrees for the reasons above that Sonderman does not teach away from the claimed invention.

Applicant argues the second point

> Second, the combination of Sonderman et al and Jain et al fail to produce the claimed invention and is improper.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Sonderman and Jain combined teach the first principle model simulation. Sonderman teaches the device physics model, process model, and an equipment model but limits the details of models to be based on the physical attributes (Col.5 Lines 47—Col.6 Line 16) where change in one is further affects the other. Such a connection is hard to model empirically or even semi empirically as the number of possibilities would be infinite. Jain's reference is used for first principles based modeling technique using the Mathematical Physical Engine (MPE) and does not need wafer based implementation for it be enabled for simulation purposes as presented in the Sonderman. Sonderman already provides Modeling and simulation facilities. Applicant's argument regarding establishing a prima facie case of obviousness are considered and are found to be unpersuasive.

Applicant further states that Jain's work is better understood in light of Kee patent. Examiner would like to point out Kee reference may have been used by another examiner for enablement, however is not part of the prior art used in this rejection. Jain and Kee are not co-inventors on either of the Kee or Jain references respectively and Examiner finds the arguments moot in view of current rejection.

Response to Applicant's Remarks for 35 U.S.C. § 112¶ 2nd

7. Claim 1-44 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 1

Examiner withdraws the rejection to claims 1-44.

Response to Applicant's Remarks for 35 U.S.C. § 101

8. Applicant arguments relating to Ex parte Lundgren are not germane to the arguments made here as no rejection was made under "technological arts" test. Further, interim guidelines may leave the issue of tangibility to open to comments as indicated by applicant, however the current office policy is to reject all claims directed to "transmission media" as an embodiment of the invention as non-statutory. The current 35 USC 101 rejection is maintained.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claim 1-47 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Exact details of what basic physical and chemical attribute of the semiconductor processing tool are used to construct a first principle simulation model which is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Applicant has argued that the meaning of the basic physical and chemical attribute of the semiconductor-processing tool is discernable to one of ordinary skill in the art. Although, teaching in the Maeda reference is present in exemplary format of molding tool, it is not there for a semiconductor-processing tool and does showing the physical and chemical attribute of the semiconductor-processing tool. Further, neither claim not the disclosure presents physical and chemical attribute of the semiconductor-processing tool in form of the first principles models. Examiner requests the applicant to provide an exact support in disclosure for such attributes in the model.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10. Claims 44 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 44 discloses "computer readable medium" which is defined in the specification (Pg.32-33 [00103] Line1-9) to include tangible items ("non volatile media" and "volatile media") and items that are non-tangible ("transmission media"). Therefore the claim as whole is not directed towards a tangible medium. One possible suggested way to overcome this rejection is to replace "computer readable medium" with "non volatile media" and "volatile media". Transmission media (Carrier wave) is understood be non-statutory and rejected under current office practice.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. **Claim 1 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/673,501.**

Application No. 10/673,583	Application No. 10/673,501
A method of facilitating a process performed by a semiconductor processing tool, comprising:	A method of facilitating a process performed by a semiconductor processing tool, comprising:
inputting data relating to a process performed by the semiconductor processing tool;	inputting data relating to a process performed by the semiconductor processing tool;
inputting a first principles physical model relating to the semiconductor processing tool;	inputting a first principles physical model relating to the semiconductor processing tool;
performing first principles simulation *for the actual process being performed* using the input data and the physical model to provide a virtual sensor measurement relating to the process performed by the semiconductor processing tool; and	performing first principles simulation *for the actual process being performed* using the input data and the physical model to provide a simulation result for the process performed by the semiconductor processing tool; and
using the virtual sensor measurement to facilitate the process performed by the semiconductor processing tool.	using the simulation result as part of a data set that characterizes the process performed by the semiconductor processing tool.

Although the conflicting claims are not identical, they are not patentably distinct from each other because both the virtual sensor measurements are the same simulation result

(Specification: Page 13[0051] Last sentence). Further, the process of facilitating could be a characterization the semiconductor fabrication process (Specification: Page 6[0032] Lines 1-5). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

2. **Claim 1 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/673,507.**

Application No. 10/673,583	Application No. 10/673,507
A method of facilitating a process performed by a semiconductor processing tool, comprising:	A method of controlling a process performed by a semiconductor processing tool, comprising:
inputting data relating to a process performed by the semiconductor processing tool;	inputting data relating to a process performed by the semiconductor processing tool;
inputting a first principles physical model relating to the semiconductor processing tool;	inputting a first principles physical model relating to the semiconductor processing tool;
performing first principles simulation *for the actual process being performed* using the input data and the physical model to provide a virtual sensor measurement relating to the process performed by the semiconductor processing tool; and	performing first principles simulation *for the actual process being performed* using the input data and the physical model to provide a first principles simulation result; and
using the virtual sensor measurement to facilitate the process performed by the semiconductor processing tool.	using the first principles simulation result to control the process performed by the semiconductor processing tool..

Although the conflicting claims are not identical, they are not patentably distinct from each other because both the virtual sensor measurements are the same simulation result (Specification: Page 13[0051] Last sentence). Further, the process of facilitating is also same as providing the simulation results to control the actual semiconductor processing tool. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

3. **Claim 1 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/673,138.**

Application No. 10/673,583	Application No. 10/673,138
A method of facilitating a process performed by a semiconductor-processing tool, comprising:	A method of facilitating a process performed by a semiconductor-processing tool, comprising:
inputting data relating to a process performed by the semiconductor processing tool;	inputting data relating to a process performed by the semiconductor processing tool;
inputting a first principles physical model relating to the semiconductor processing tool;	inputting a first principles physical model relating to the semiconductor processing tool;
performing first principles simulation *for the actual process being performed* using the input data and the physical model to provide a virtual sensor measurement relating to the process performed by the semiconductor processing tool; and	performing first principles simulation *for the actual process being performed* using the input data and the physical model to provide a first principles simulation result; and
using the virtual sensor measurement to facilitate the process performed by the semiconductor processing tool.	using the first principles simulation result to facilitate the process performed by the semiconductor processing tool.

Although the conflicting claims are not identical, they are not patentably distinct from each other because both the virtual sensor measurements are the same simulation result (Specification: Page 13[0051] Last sentence). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Further, all the three non-statutory obviousness-type double patenting rejections for the application have substantially same or identical specification. Also, independent claims belonging different statutory category, having substantially similar limitations, in the three co-pending applications may also have similar double patenting rejections.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. Claims 1-11, 13-14, 17-19, 21-27, 28-32, 33-38, 40-41, 44-46, 48-54, 55-57 and 60-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter).

Jain Reference has been provided with the previous office action.

Regarding Claim 1

Sonderman teaches a method to facilitate a process performed by a semiconductor-processing tool (Sonderman: Summary, at least in Col.2 Lines 10-17;Col.3 Lines 45-49) by inputting process data relating to the actual process performed by the semiconductor-processing tool (Sonderman: at least in Col.3 Lines 50-67; Col.7 Lines 8-20). Further, Sonderman teaches inputting the first principle physical model relating to the semiconductor-processing tool describing at least one of a basic physical or chemical attributes (Sonderman: at least in Col.5 Lines 11-17; 49-67) as device physics model, a process model and an equipment model. Further, Sonderman teaches performing first principle simulation *for the actual process being performed (Sonderman: Col.7 Lines 4-7; Col.3 Lines 56-63)* using the input data and the physical model to provide virtual sensor measurements relating to the process performed by the semiconductor–processing tool (Sonderman: at least in Col.5-7). Further, Sonderman teaches using the virtual sensor measurements to facilitate the *actual* process *being* performed by the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 48-64; Fig.1-8; Col.7 Lines 37-65).

Sonderman does not teach first principle model including a set of computer encoded differential equations.

Jain teaches computer encoded differential equations using MPE engine, which can be applied to wafer processing (Jain: Abstract). Jain also teaches dedicated and wafer level implementation of MPE engine to provide enhanced performance (Jain: Pg. 372 Section V Dedicated MPE).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Jain to Sonderman to solve differential equation for the semiconductor processing tool. Sonderman teaches building various models, which work in real-time feedback control simulating actual semiconductor modeling process (Sonderman: Fig.1; *Col.7 Lines 8-20*), while Jain makes possible by providing model-solving capacity in real time when differential equations are present in the model (like thermal patterns in semiconductor wafer model) (Jain: Abstract).

Regarding Claim 2

Sonderman teaches directly inputting the *process* data relating to the *actual* process performed by the semiconductor-processing tool from at least one of physical sensor (eg. Scatterometry data, overlay data, dimensional data) and a metrology tool physically mounted on the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 31-48; Col.4-8; Fig.1, 7; *Col.7 Lines 8-20*).

Regarding Claims 3-5

Sonderman teaches indirectly inputting the *process* data relating to the *actual* process performed by the semiconductor-processing tool from one of the manual input devices and a database as manual fashion data retrieval and automatic data retrieval; inputting data recorded from the previous run; inputting the data set by a simulation operator ((Sonderman: at least in Fig.1-3 Col.1; Col.4-7).

Regarding Claims 6-9

Sonderman teaches inputting *process* data relating to at least one of the physical characteristics of the semiconductor-processing tool and semiconductor tool environment, data relating to at east on of the characteristics and a result of a process performed by the semiconductor processing tool; inputting a spatially resolved model (as modified models) of the geometry of the semiconductor processing tool; inputting fundamental equations necessary to perform first principle simulation for the desired simulation result (Sonderman: at least in Col.5 Lines 10-18; Col.6 Lines 48-63; Col.9 (equations); Col.5-9; Fig 1-3).

Regarding Claim 10

Sonderman teaches performing interaction concurrently between the simulation environment (first principle simulation) and the semiconductor-processing tool (Sonderman: Fig.2; Col.4 Lines 48-63).

Regarding Claim 11

Sonderman teaches repeating the step of inputting the data from (physical sensor) metrology tool into first principle simulation and facilitating the semiconductor

process concurrently with running the semiconductor process based on virtual sensor measurements obtained during the semiconductor process (Sonderman: at least in Col.4 Lines 48-Col.5 Lines 10; Col.7 Lines 36-53; col.4-7).

Regarding Claims 13-14

Sonderman teaches performing first principle simulation not concurrently with the process performed; inputting data from at least one initial condition recorded from a previous process performed (Sonderman: at least in Col.5-8; Fig.3-4).

Regarding Claim 17

Sonderman teaches using virtual sensor measurements to characterize the semiconductor-processing tool (Sonderman: at least in Col.5 Lines 11-17; equipment model).

Regarding Claim 18

Sonderman teaches using virtual tool measurements to control the process performed by the semiconductor-processing tool (Sonderman: at least in Col.5 Lines 41-47).

Regarding Claim 19

Sonderman teaches using virtual sensor measurements to detect a fault in the process performed by the semiconductor-processing tool (Sonderman teaches: at least in Col.7, Fig 5-6).

Regarding Claims 21-25

Sonderman teaches using a network of interconnected resources to perform at least one of the process steps recited in claim 1; using code parallelization among

interconnected computational resources to share the computational load of the first principle simulation; sharing simulation information among the interconnected resources to facilitate a process by the semiconductor-processing tool; sharing simulation results among the interconnected resources to reduce redundant execution of substantially similar first principle simulation by different resources; sharing information comprising model changes among the interconnected resources to reduce the redundant refinements of first simulation by different resources (Sonderman: Fig.1-3, computer code software is described in Col.9 Lines 58 onward; Col.5-8).

Regarding Claims 26-27

Sonderman teaches remote access to computational and storage resources (Sonderman: Col.9 Line 58-Col.10 Line 31) where in wide area network is art inherent.

Regarding Claim 28

System claim 28 discloses substantially similar limitations as method claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 29

System claim 29 discloses substantially similar limitations as method claim 2 and is rejected for the same reasons as claim 2.

Regarding Claims 30-32

System claims 30-32 disclose substantially similar limitations as method claims 3-5 and are rejected for the same reasons as claims 3-5.

Regarding Claims 33-36

System claims 33-36 disclose substantially similar limitations as method claims 6-9 and are rejected for the same reasons as claims 6-9.

Regarding Claim 37

System claim 37 discloses substantially similar limitations as method claim 10 and is rejected for the same reasons as claim 10.

Regarding Claim 38

System claim 38 discloses substantially similar limitations as method claim 11 and is rejected for the same reasons as claim 11.

Regarding Claims 40-41 and 61

System claims 40-41 and 61 disclose substantially similar limitations as method claims 13-14 and are rejected for the same reasons as claims 13-14.

Regarding Claim 44

System claim 44 discloses substantially similar limitations as method claim 17 and is rejected for the same reasons as claim 17.

Regarding Claim 45

System claim 45 discloses substantially similar limitations as method claim 18 and is rejected for the same reasons as claim 18.

Regarding Claim 46

System claim 46 discloses substantially similar limitations as method claim 19 and is rejected for the same reasons as claim 19.

Regarding Claims 48-52

System claims 48-52 disclose substantially similar limitations as method claims 21-25 and are rejected for the same reasons as claims 21-25.

Regarding Claims 53-54

System claims 53-54 disclose substantially similar limitations as method claims 26-27 and are rejected for the same reasons as claims 26-27.

Regarding Claim 55

System claim 55 discloses substantially similar limitations as method claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 56

System claim 56 discloses substantially similar limitations as method claim 10 and is rejected for the same reasons as claim 10.

Regarding Claim 57

System claim 57 discloses substantially similar limitations as method claim 11 and is rejected for the same reasons as claim 11.

Regarding Claim 60

System claim 60 discloses substantially similar limitations as method claim 22 and is rejected for the same reasons as claim 22.

Regarding Claim 62

System claim 62 discloses substantially similar limitations as method claim 1 and is rejected for the same reasons as claim 1.

Regarding Claims 63-65

Jain teaches use of Navier Stokes and other known simulation solutions for solving various simulation problems as initial condition (Jain: Pg. 367-368 Section "Governing Rationale" Sub-Section A. Governing Equations). Sonderman also teaches initializing the models with input data (Sonderman: Col.7 Lines 8-20).

12. Claims 12, 15-16, 20, 39, 42-43, 47, 58-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter), further in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter).

Regarding Claim 12

Teachings of Sonderman & Jain are disclosed in claim 1 rejection above. Sonderman teaches setting boundary condition for first principle simulation through the process parameters (Sonderman: at least in Col.5-6).

Sonderman & Jain do not teach performing time dependent concurrent simulation without direct input from semiconductor process to facilitate semiconductor process based on virtual sensor measurement.

Chen teaches time dependent concurrent simulation without direct input from semiconductor process and applies the result to facilitate the semiconductor process concurrently with running the semiconductor process based on virtual sensor measurements obtained during the semiconductor process. Chen teaches simulation based on the statistical data, which in turn provides the output to actual fabrication process (Chen: at least in Col.3 Lines 12-18).

Motivation to combine Jain to Sonderman is provided above in claim 1 rejection.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Chen to Sonderman. The

motivation to combine would have been that Chen and Sonderman both are analogous art concerned with simulating the semiconductor fabrication process and providing the best control parameters to the actual semiconductor-processing tool (Chen: at least in Col.3 Lines 19-23). Chen facilitates in building the process model that can be run in parallel to actual process thereby providing more specific embodiment to Sonderman's teachings (Chen: Col.3 Lines 12-24).

Regarding Claim 15

Chen teaches indirectly putting best-known input parameters for the physical model (Chen: at least in Col.3 Lines 19-23).

Regarding Claim 16

Chen teaches comparing virtual sensor measurements with the actual sensor measurements and refining at least one best known input parameters and the physical model to obtain better agreement between the virtual sensor measurements with actual sensor measurements (Chen: at least in Col.3 Lines 48-57; Calibrate run calibrate simulated).

Regarding Claim 20

Chen teaches storing virtual sensor measurement in a library for subsequent use in a first principle simulation (Chen: at least in Col.3; Specifically in Col.3 Lines 37-41).

Regarding Claim 39

System claim 39 discloses substantially similar limitations as method claim 12 and is rejected for the same reasons as claim 12.

Regarding Claim 42

System claim 42 discloses substantially similar limitations as method claim 15 and is rejected for the same reasons as claim 15.

Regarding Claim 43

System claim 43 discloses substantially similar limitations as method claim 16 and is rejected for the same reasons as claim 16.

Regarding Claim 47

System claim 47 discloses substantially similar limitations as method claim 20 and is rejected for the same reasons as claim 20.

Regarding Claim 58

System claim 58 discloses substantially similar limitations as method claim 12 and is rejected for the same reasons as claim 12.

Regarding Claim 59

System claim 59 discloses substantially similar limitations as method claim 16 and is rejected for the same reasons as claim 16.

Conclusion

13. All claims are rejected.

14. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Akash Saxena
Patent Examiner, GAU 2128
(571) 272-8351
Friday, September 01, 2006

Kamini S. Shah
Supervisory Patent Examiner, GAU 2128
Structural Design, Modeling, Simulation and Emulation